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(54) Abstract Title
Iterative (turbo) equalisation

(57) There is disclosed a method of recovering a received signal comprising the steps of: equalising (100) the received signal, channel decoding (102) the equalised received signal, wherein a priori information of the received signal is utilised in the equalisation step. The equalising step may be performed in a sub-optimum equaliser. The channel decoding step may be performed in an a posterior channel decoder. The a priori information is obtained by subtracting (110) the output of the a posterior decoder (102) from the output of the deinterleaver (104).

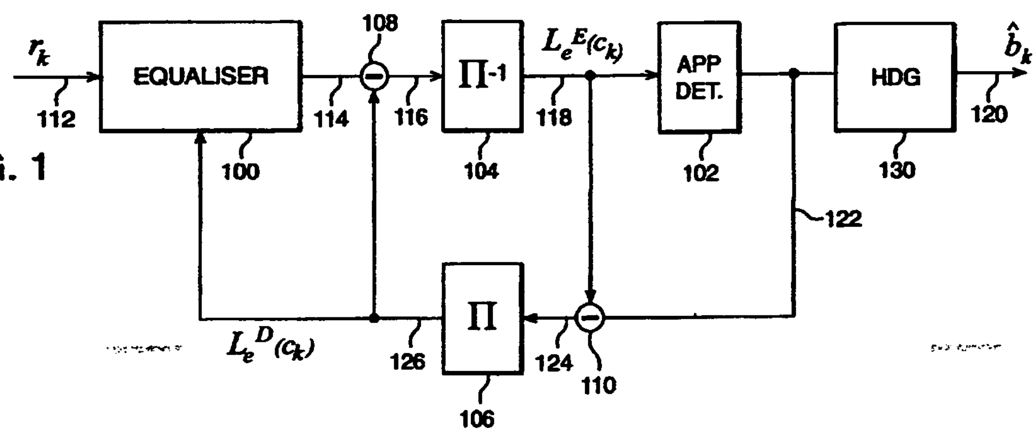

FIG. 1

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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

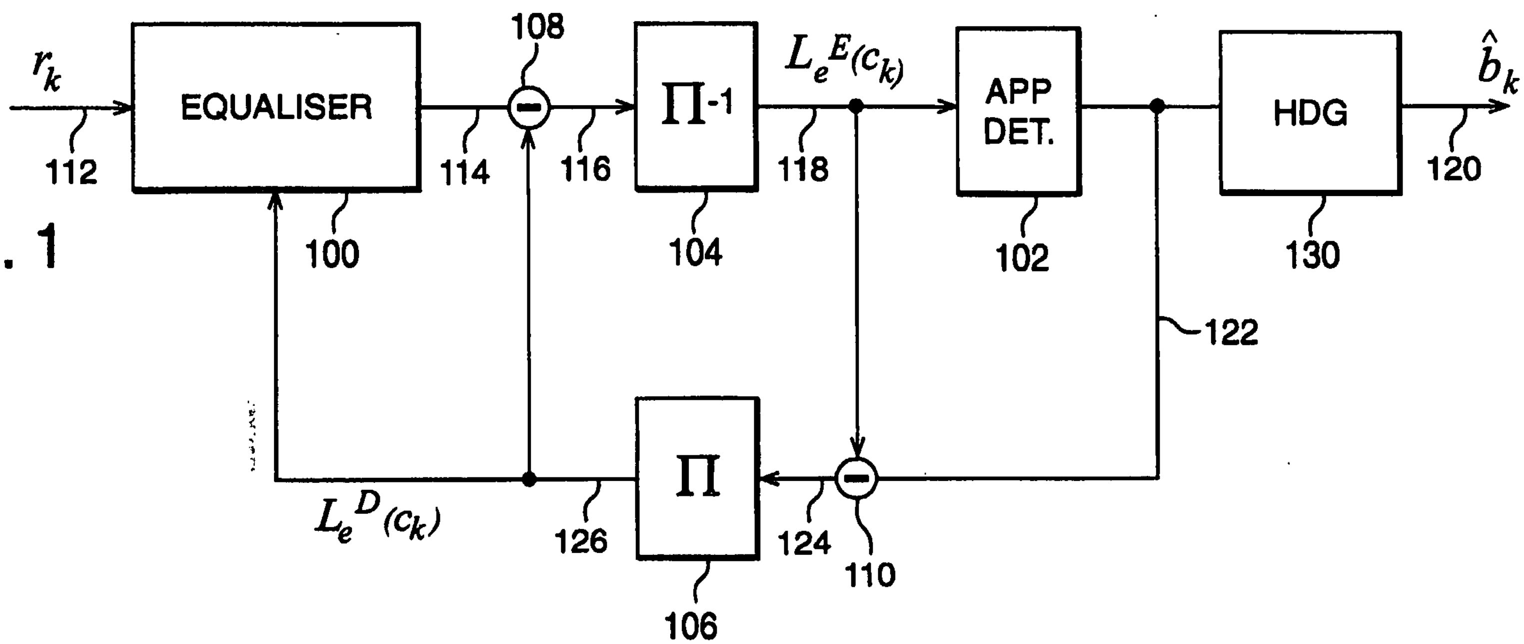

r_k
112
EQUALISER
100
114
108
116
Π^{-1}
104
$L_e^E(c_k)$
118
APP DET.
102
HDG
130
$\hat{b}_k$
120
122
110
124
Π
106
126
$L_e^D(c_k)$

FIG. 1

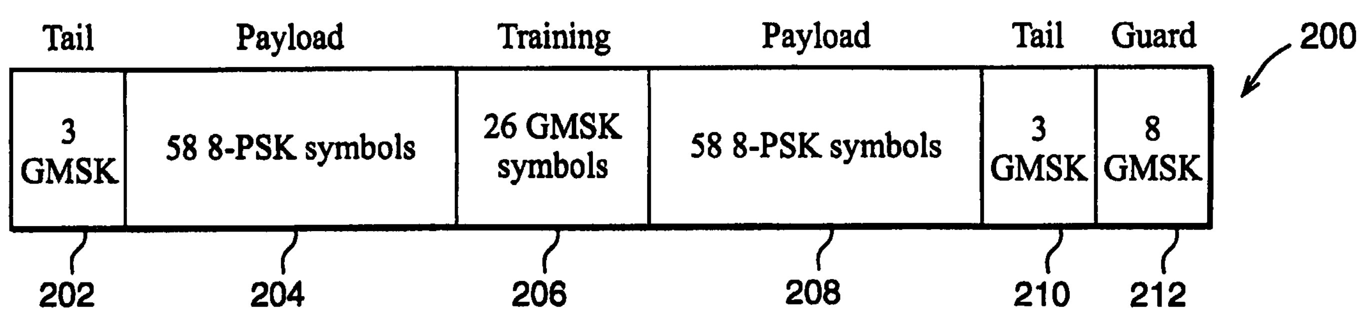

Tail
Payload
Training
Payload
Tail
Guard
3 GMSK
58 8-PSK symbols
26 GMSK symbols
58 8-PSK symbols
3 GMSK
8 GMSK
200
202
204
206
208
210
212

FIG. 2

FIG. 3

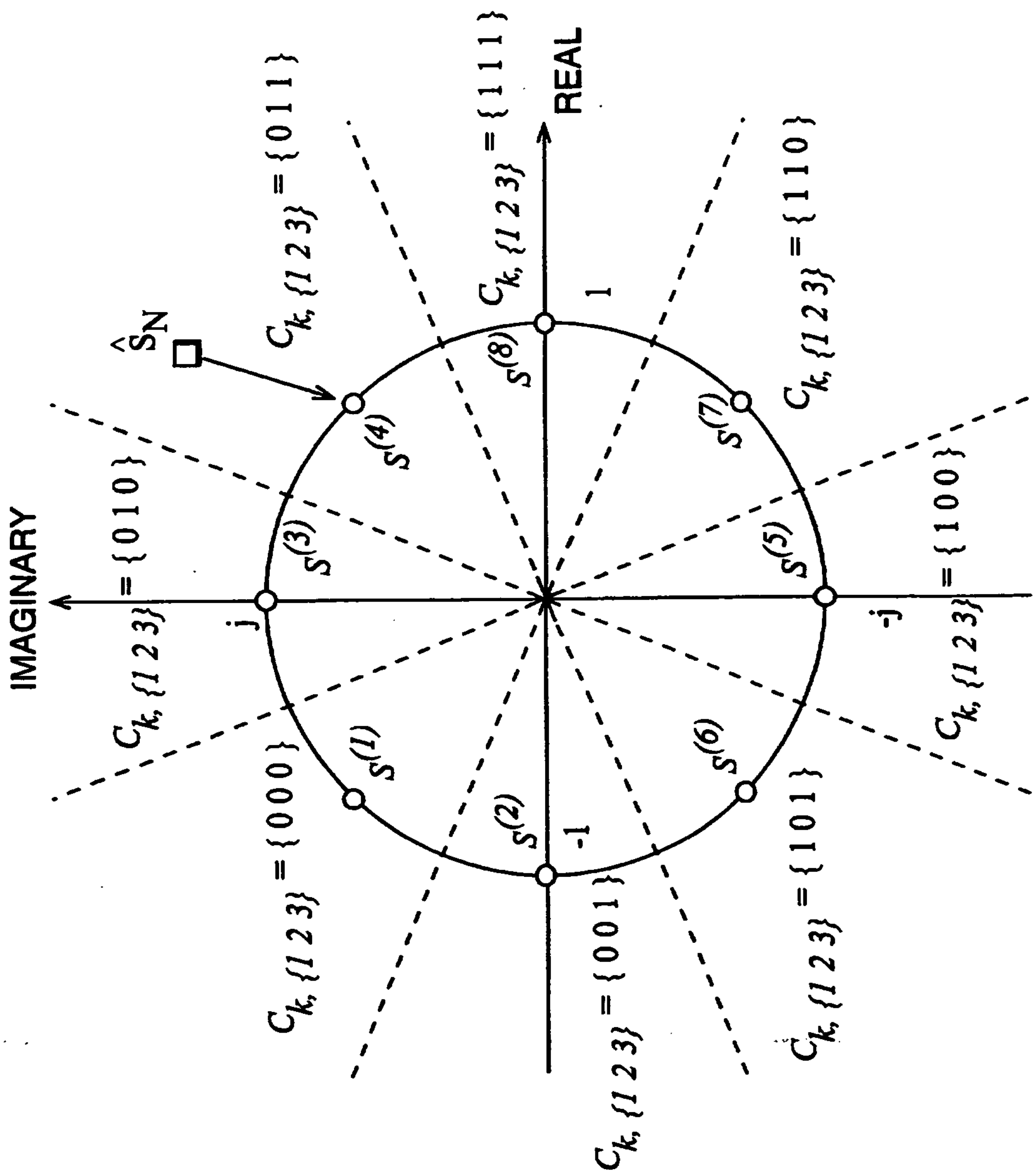
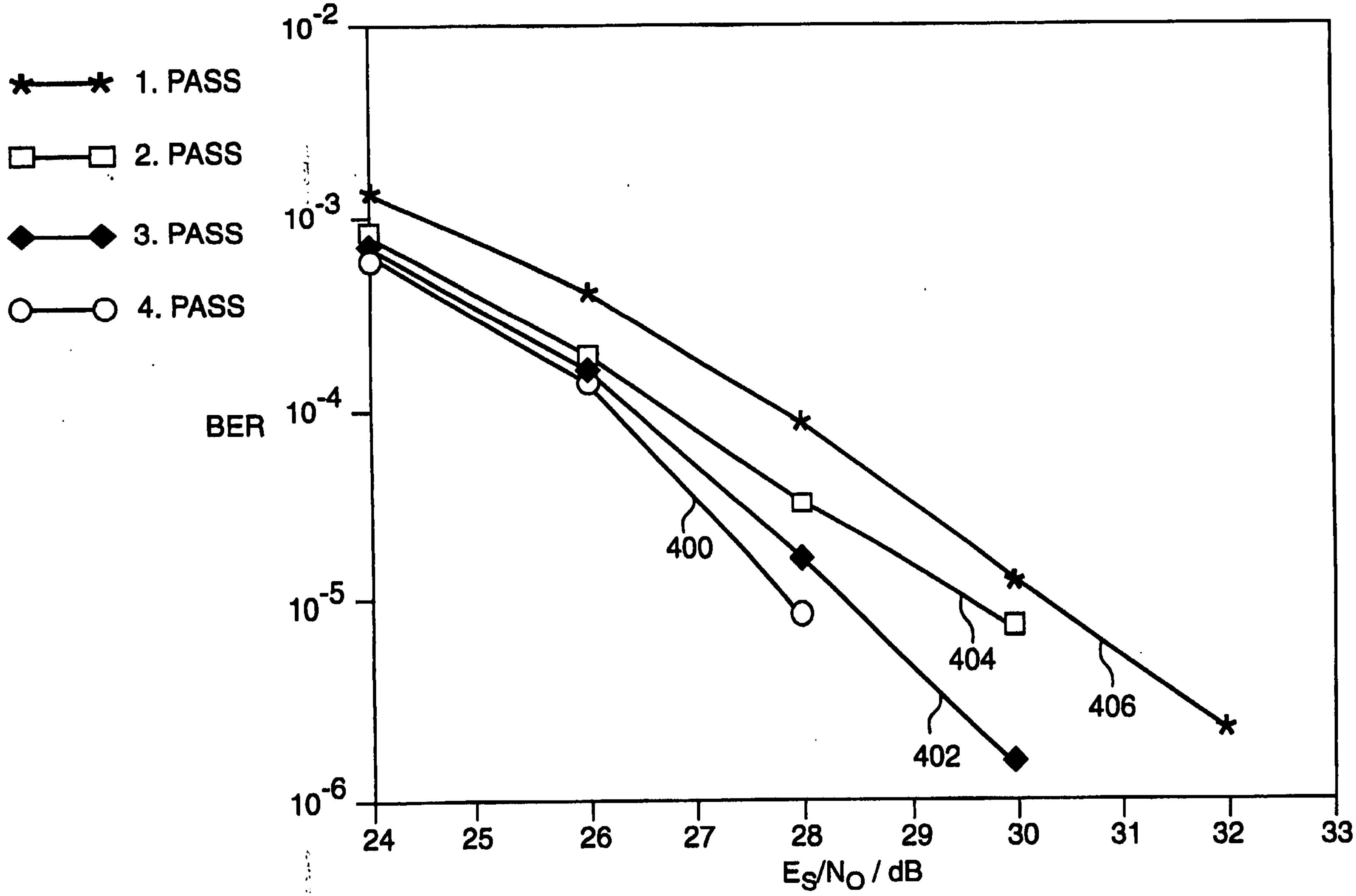

IMAGINARY
REAL
$\hat{S}_N$
j
-j
1
-1
$S^{(1)}$
$S^{(2)}$
$S^{(3)}$
$S^{(4)}$
$S^{(5)}$
$S^{(6)}$
$S^{(7)}$
$S^{(8)}$
$C_{k,\{1\,2\,3\}} = \{0\,0\,0\}$
$C_{k,\{1\,2\,3\}} = \{0\,0\,1\}$
$C_{k,\{1\,2\,3\}} = \{0\,1\,0\}$
$C_{k,\{1\,2\,3\}} = \{0\,1\,1\}$
$C_{k,\{1\,2\,3\}} = \{1\,0\,0\}$
$C_{k,\{1\,2\,3\}} = \{1\,0\,1\}$
$C_{k,\{1\,2\,3\}} = \{1\,1\,0\}$
$C_{k,\{1\,2\,3\}} = \{1\,1\,1\}$

FIG. 4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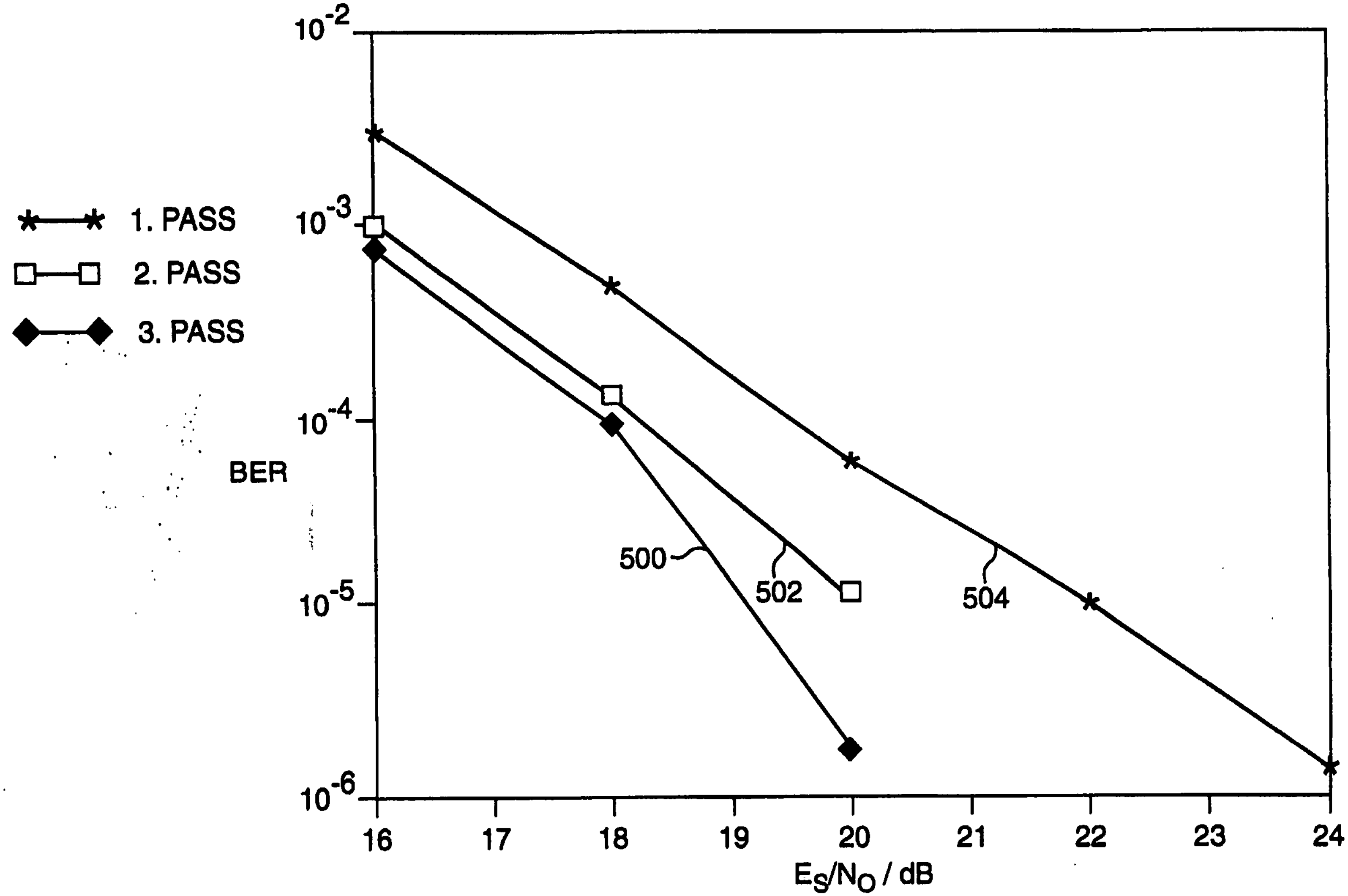
2. PASS
3. PASS
4. PASS
BER
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
24
25
26
27
28
29
30
31
32
33
E_S/N_O / dB
400
402
404
406

FIG. 5



1. PASS
2. PASS
3. PASS
BER
10-2
10-3
10-4
10-5
10-6
500
502
504
16
17
18
19
20
21
22
23
24
Es/No / dB

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TURBO EQUALIZATION WITH A DECISION FEEDBACK EQUALIZER

Field of the Invention

The invention relates to so-called turbo decoders, and particularly but not exclusively to the use of turbo decoders in the receivers of communication systems utilising non-binary symbol alphabets.

Background to The Invention

In a digital communication system the data bits are encoded at the transmitter to protect the transmitted data against noise and fading. The data is transmitted over a frequency selective channel which causes inter-symbol interference (ISI). Therefore, it is necessary to equalize the impairments of the radio propagation channel. At the receiver the received data is equalized and decoded. The equalizer eliminates inter-symbol interference (ISI) caused by multi-paths in the communication channel.

An optimum receiver utilises a joint maximum likelihood scheme, where equalization and decoding are performed jointly. An optimum receiver use trellis equalisers. Trellis equalizers which provide optimum performance, such as *a posteriori* probability (APP) detectors, require an excessive number of states in the trellis when the symbol alphabet is non-binary. Such an optimum receiver therefore becomes too complex to implement in communication systems utilising non-binary symbol alphabets.

An 8-PSK modulation scheme is proposed by ETSI to increase the data rates in a GSM system. An 8-PSK modulation scheme with a number of channel taps $K = 5$ requires a trellis of $8^{5-1} = 4096$ states. It is not possible to implement such an optimum equalizer using current digital signal processing (DSP) technology.

Therefore, sub-optimum reduced state or linear equalizers have to be used.

Iterative equalization and decoding, known as 'Turbo equalization', in a receiver for digital communication has been shown to increase the performance of a receiver in terms of bit error rates (BER). Turbo

equalisation iteratively detects and decodes coded data transmitted over a frequency selective channel.

Iterative equalization and decoding attempts to come close to the optimum joint strategy by performing equalization and decoding several times in series.

The Turbo equalisation principle has been used in many applications. C.Berrou, A.Glavieux, and P.Thitimajshima, "Near Shannon limit error-correcting and decoding: Turbo codes (1)", ICC, pp.1064-1070, May 1993 discloses an application in iterative de-mapping. S.ten Brink, J.Speidel, and R.Yan, "Iterative demapping and decoding for multilevel modulation", GLOBECOM'98, pp.2950-2955, Dec. 1998 discloses an application in multi-user detection. S.Benedetto, D.Divsalar, G.Montorsi, and F.Pollara, "Self-concatenated trellis coded modulation with self-iterative decoding", GLOBECOM'98, pp.2956-2962, Dec. 1998 discloses an application in trellis coded modulation schemes.

It is an object of the present invention to provide an improved implementation of a turbo decoder, namely a decoder in which equalisation and channel decoding are performed iteratively.

Summary of the Invention

According ot the present invention there is provided a method of recovering a received signal comprising the steps of: equalising the received signal, channeld decoding the equalised received signal, wherein *a priori* information of the received signal is utilised in the equalisation step..

The equalising step may be performed in a sub-optimum equaliser.

The channel decoding step may be performed in an *a posterior* channel decoder.

The a priori information may be generated in dependence on the channel decoded received signal.

The transmitted signal may be recovered in a series of iterations.

In a first iteration the received signal may be decoded without any *a priori* information. In n subsequent iterations the received signal may be

equalised using *a priori* information generated in the previous iteration. After the (n+1)th iteration a hard decision for the received signal may be generated.

After the equalisation step the *a priori* information may be removed from the equalised signal before channel decoding.

The *a priori* information may be generated by subtracting the input of the channel decoder from the output of the channel decoder.

The received signal may be de-interleaved after equalisation.

The method of claim 11, wherein the *a priori* information is interleaved prior to equalisation.

The invention also provides a method of recovering a transmitted signal comprising the steps of: in a first iteration: equalising the received signal in a sub-optimum equaliser; channel decoding the equalised received signal in an *a posterior* channel decoder; generating *a priori* information in dependence on the channel decoded received signal; for the subsequent n iterations: equalising the received signal in the sub-optimum equaliser utilising the a priori information from the previous iteration; adjusting the equalised received signal by removing the a priori information therefrom; channel decoding the adjusted equalised received signal; wherein after the (n+1)th iteration a hard decision is determined based on the adjusted equalised received signal.

According to the present invention there is also provided circuitry for recovering a transmitted signal comprising: an equaliser for equalising the received signal; a channel decoder connected to the output of the equaliser for channel decoding the received signal; and circuitry for generating a priori information of the received signal, wherein said *a priori* information forms an input to the equaliser.

The equaliser may be a sub-optimum equaliser.

The channel decoder may be an *a posterior* channel decoder.

The circuitry for generating the *a priori* information may receive as an input the output of the channel decoder.

The circuitry may further comprise a first subtractor, wherein the first subtractor subtracts the *a priori* information at the output of the circuitry for generating the *a priori* information from the output of the eqauliser, the output of the subtractor forming the input to the channel decoder.

The circuitry for generating the *a priori* information may include a second subtractor, the second subtractor being connected to subtract the signal at the output of the channel decoder form the signal at the input of the channel decoder, the output of the second subtractor forming the output of the circuitry for generating the *a priori* information.

The circuitry may further comprise de-interleaving circuitry connected to de-interleave the output of the equaliser.

The circuitry of may further comprise interleaving circuitry connected to interleave the input of the equaliser.

The circuitry may be controlled to perform a series of iterations on the received signal.

The equaliser may receive a signal from the circuitry for generating the a priori information on the second and subsequent iterations.

The invention also provides a Turbo equaliser for recovering a transmitted signal comprising: a sub-optimum equaliser connected to receive as a first input the received signal and as a second input a priori information associated with the received signal, and for outputting a *a priori* equalised received signal; circuitry, connected to receive as a first input the equalised received signal and as a second input the a priori information, and for removing the a priori information from the equalised received signal, and for generating an equalised received signal; an *a posterior* channel decoder connected to receive as an input the equalised received signal and for outputting a channel decoded received signal; means connected to receive as a first input the equalised received signal and as a second input the channel decoded received signal, and for outputting the a priori information; and a hard decision genarator having an input connected to the output of the channel decoder and an output, wherein on a first iteration of the Turbo decoder there is no *a priori* information, and

wherein on the nth iteration the hard decision on the output of the hard decision generator is obtained.

Performing iterative equalization and decoding with a sup-optimum equalizer results in improved performance of a receiver in terms of BER. In accordance with the present invention, a decision feedback equalizer incorporates *a priori* information.

A priori information in the decision feedback equalizer helps to combat error propagation and residual inter-symbol interference.

The invention incorporates a priori information from the channel decoder within a non-probabilistic equalizer. The MMSE-BDFE and a soft-output channel decoder exchange extrinsic information on the coded bits in an iterative way.

The invention preferably utilizes the Turbo equalisation principle for iterative equalization and decoding.

Brief Description of the Drawings

Figure 1 illustrates a block diagram of receiver circuitry for iteratively detecting symbols and decoding bits using turbo equalisation;

Figure 2 illustrates a burst structure for EDGE;

Figure 3 illustrates an 8-PSK constellation with an example of a hard decision;

Figure 4 and 5 illustrate simulation results.

Description of the Preferred Embodiment

The invention is described in relation to a preferable implementation of a mobile time division multiple access (TDMA) communication system. A TDMA system is a GSM-like system where the payload is modulated by 8-PSK. This is a likely scenario for the evolution of the current GSM system (EDGE - enhanced data rate for GSM evolution) in order to increase the data rates.

The invention will be described herein with reference to an exemplary implementation of a turbo equaliser in a Minimum Mean Square Error - Block Decision Feedback Equalizer (MMSE-BDFE). This equaliser is a

non-probabilistic equaliser, and is chosen for the exemplary implementation because of its simplicity and good performance.

In mobile communications the radio channel can be modelled by a tapped delay line with time varying coefficients. This finite impulse response (FIR) channel model can be seen as a convolutional encoder with rate 1. Therefore, it is possible to treat the channel encoder and the channel itself as a serial concatenation of two encoders. At the receiver the serially concatenated `coding` scheme can be iteratively decoded by a decoder such as is shown in Figure 1.

The receiver of Figure 1 comprises a Minimum Mean Square Error - Block Decision Feedback Equalizer (MMSE-BDFE) forming an equaliser block 100, a channel decoder comprising an *a posterior* probability decoder 102, a de-interleaver 104, an interleaver 106, first and second subtractors 108 and 110, and a hard decision generator 130.

The received signal is received on line 112 and forms a first input to the equaliser block 100. A second input to the equaliser block 100 is formed by the output of the interleaver 106. The output of the equaliser block 100 on line 114 forms a first input to the subtractor 108. A second input to the subtractor 108 is formed by the output of the interleaver 106. The output of the subtractor on line 116 forms the input to the de-interleaver 104. The output of the de-interleaver 104 on line 118 forms an input to the subtractor 110 and the channel decoder 102. The output of the channel decoder on line 122 forms a second input to the subtractor 110, and an input to the hard decision generator 130. The subtractor 124 generates an output on line 124 which forms an input to the interleaver 106. The hard decision generator 130 has an output on line 120.

In a first detection pass or iteration there is no *a priori* information from the channel decoder 102 available to the equaliser 100. The equalizer detects the symbols in the received signal on line 112, and converts the symbols into soft values of the coded bits c_k at time instant k. The soft values are conventionally known as L-values, and are defined as follows

$$L^{E}(c_k) = \log \frac{\Pr(c_k = +1)}{\Pr(c_k = -1)} \qquad (1)$$

The soft values are generated at the output of the equaliser on line 114. In the first iteration no a priori information is available, and the subtractor 108 therefore subtracts zero from the output of the equaliser. Thus on the first iteration, the input to the de-interleaver on line 116 corresponds to the output of the equaliser on line 114.

After de-interleaving of the coded bits, the *a posterior* probability (APP) channel decoder receives the coded bits $L_e^E(c_k)$on line 118. At each decoding stage, i.e. each iteration, the *a posterior* probability channel decoder provides soft values, or L-values, on the coded bits and on the information bits. These soft values are generated on line 122.

The L-values on the coded bits are fed back to the equalizer.

In order to feed back independent information, the L-values from the *a posterior* probability channel decoder on line 110 have to be first subtracted by the L-values from the equalizer on line 118, in the subtractor 110. This new information on line 124 is called extrinsic information, and is denoted by $L_e^D(c_k)$.

The extrinsic information on line 124 is then interleaved in the interleaver 106, and the interleaved extrinsic information is presented on line 126 for use by the equaliser block in the second and subsequent iterations.

In the detection process of the equalizer this extrinsic information is used in the second and subsequent iterations as *a priori* information. By feeding back the *a priori* information from the channel decoder, the equaliser makes more reliable decisions to produce more reliable soft value results, and as a result there are less errors.

On the second and subsequent iterations, the a priori information on line 126 is subtracted from the output of the equalsier on line 114 by the subtractor 108, and the adjusted value on line 116 is de-interleaved and provided to the channel decoder 102.

The extrinsic information from the equalizer $L_e^E(c_k)$ is then again processed by the channel decoder 102.

The extrinsic information $L_e^E(c_k)$ can be scaled down by a factor γ. Due to the imperfections (e.g. residual ISI) of the MMSE-BDFE, the soft values tend to be too optimistic. Empirical values of γ range between 0.01 and 0.5 .

This operation of equalising and channel decoding is repeated for a determined number of iterations, and after a determined number of iterations n hard decisions are made. On the n^{th} iteration the soft values on the information bits from the channel decoder on line 122 are sliced to obtain the hard decisions designated by $\hat{b}_k$ on line 120.

A theoretical analysis of the operation of the decoder of Figure 1 is given hereinbelow.

In a TDMA system the data is transmitted in bursts. An example of a TDMA burst proposed for use in EDGE is shown in Figure 2, and contains 2 blocks of data 204 and 208, tail 202 and 210, a training symbol 206 and a guard symbol 212.

The received burst of data at the input of the receiver can be written as

$$\mathbf{r} = \mathbf{Hs} + \mathbf{n} \tag{2}$$

where $\mathbf{s}$ represents the transmitted symbols, $\mathbf{H}$ represents the channel matrix, and $\mathbf{n}$ represents the Additive White Gaussian Noise (AWGN). The minimum mean square error (MMSE) solution to obtain the estimated symbols $\hat{\mathbf{s}}$ is:

$$\hat{\mathbf{s}} = (\mathbf{H}^H\mathbf{H} + 2\sigma^2\mathbf{I})^{-1}\mathbf{H}^H\mathbf{r} \tag{3}$$

where σ^2 is the variance of the Additive White Gaussian Noise in in-phase and quadrature component, and $\mathbf{I}$ denotes the identity matrix. This relationship can be found in A.Klein, G.Kaleh, and P.Baier, "Zero forcing and minimum mean-square-error equalization for multiuser detection in code-division multiple-access channels", IEEE Trans. on Vehicular Technology, vol.45, pp.276-287, May 1996.

The Cholesky factorization can be used to split the MMSE equalizer into two parts: a feed-forward part and a feedback part. The filter of the feed-forward part is a whitening matched filter, and the filter of the feedback part cancels the postcursor ISI. The factorization process can be expressed as follows:

$$\mathbf{U}^H\mathbf{U} = (\mathbf{H}^H\mathbf{H} + 2\sigma^2\mathbf{I}) \tag{4}$$

where $\mathbf{U}$ is an upper triangular matrix, and hence $\mathbf{U}^H$ is a lower triangular matrix. Combining equations (3) and (4) results in:

$$\mathbf{U}^H\mathbf{U}\hat{\mathbf{s}} = \mathbf{H}^H\mathbf{r} \tag{5}$$

Therefore, letting $\mathbf{y} = \mathbf{U}\hat{\mathbf{s}}$

$$\mathbf{U}^H\mathbf{y} = \mathbf{H}^H\mathbf{r} \tag{6}$$

Equation (6) is easily solved for $\mathbf{y}$ since $\mathbf{U}^H$ is lower triangular. The whitened matched signal $\mathbf{y}$ is still corrupted by postcursor inter-symbol interference and, therefore, the influence of previous decisions is successively subtracted out of the current estimated symbol. This subtraction can be achieved by solving the following equation recursively:

$$\mathbf{U}\hat{\mathbf{s}} = \mathbf{y} \tag{7}$$

which can be represented as full matrices as follows:

$$\begin{bmatrix} U_{1,1} & \cdots & U_{1,N-1} & U_{1,N} \\ \vdots & \ddots & \vdots & \vdots \\ 0 & \cdots & U_{N-1,N-1} & U_{N-1,N} \\ 0 & \cdots & 0 & U_{N,N} \end{bmatrix} \begin{bmatrix} \hat{s}_1 \\ \vdots \\ \hat{s}_{N-1} \\ \hat{s}_N \end{bmatrix} = \begin{bmatrix} y_1 \\ \vdots \\ y_2 \\ y_N \end{bmatrix}$$

where N is the length of one block containing the payload symbols $\mathbf{s}$. First a solution for the following expression is obtained:

$$\hat{s}_N = \frac{y_N}{U_{N,N}} \tag{8}$$

In order to reduce the noise and to cancel the postcursor inter-symbol interference effectively, a hard decision $\hat{s}_N^{(m)}$ is made, with $m = 1 \ldots 8$ on $\hat{s}_N$. The hard decided symbol $\hat{s}_N^{(m)}$ is obtained according to Figure 3, which

shows an 8-PSK constellation with an example of a hard decision on symbol $\hat{s}_N$, and used in the next equation (7).

$$\hat{s}_k = \frac{y_k - \sum_{n=k+1}^{N} U_{k,n} \hat{s}_n^{(m)}}{U_{k,k}} = \frac{\tilde{y}_k}{U_{k,k}} \qquad (9)$$

When making a hard decision on symbol $\hat{s}_k$, it is beneficial if *a priori* information from the channel decoder could be included. The *a posterior* probability channel decoder provides soft values on the coded bits and not on the symbols themselves. It is therefore necessary to estimate the symbol via the soft values on the coded bits. Three soft values on the coded bits $c_{k,i}; i = 1,2,3$ form a symbol $\hat{s}_k$.

The *a posteriori* probability of the coded bit $c_{k,i}$ being +1 can be written as as follows

$$\Pr(c_{k,i} = +1 \mid \tilde{y}_k) = \frac{\sum_{s_k \in S_i^{(+1)}} p(\tilde{y}_k \mid s_k) \Pr(c_{k,i} = +1)}{\sum_{s_k} p(\tilde{y}_k \mid s_k) \Pr(c_{k,i})} =$$

$$\frac{\sum_{s_k \in S_i^{(+1)}} \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\left|\tilde{y}_k - s_k U_{k,k}\right|^2 \frac{1}{2\sigma^2} \right) \Pr(c_{k,i} = +1)}{\sum_{s_k} \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\left|\tilde{y}_k - s_k U_{k,k}\right|^2 \frac{1}{2\sigma^2} \right) \Pr(c_{k,i})} \qquad (10)$$

where $S_i^{(+1)}$ denotes the set of symbols s_k for which $c_{k,i} = +1$. Using the definition of L-values from equation (1) the following expression is obtained:

$$L(c_{k,i} \mid \tilde{y}_k) = \log\left(\frac{\sum_{s_k \in S_i^{(+1)}} \exp\left(-\left|\tilde{y}_k - s_k U_{k,k}\right|^2 \frac{1}{2\sigma^2} \right)}{\sum_{s_k \in S_i^{(-1)}} \exp\left(-\left|\tilde{y}_k - s_k U_{k,k}\right|^2 \frac{1}{2\sigma^2} \right)} \right) + L_e^D(c_{k,i})$$

The well known max-log approximation $\log \sum_i a_i = \max\{\log a_i\}$ [9] may be used to write

$$L(c_{k,i} \mid \tilde{y}_k) \approx \max_{s_k \in S_i^{(+1)}} \left\{ -\left|\tilde{y}_k - s_k U_{k,k}\right|^2 \frac{1}{2\sigma^2} \right\} - \max_{s_k \in S_i^{(-1)}} \left\{ -\left|\tilde{y}_k - s_k U_{k,k}\right|^2 \frac{1}{2\sigma^2} \right\} + L_e^D(c_{k,i}) \qquad (11)$$

Now the soft value $L(c_{k,i} \mid \tilde{y}_k)$ can be sliced to obtain the hard decisions on the coded bit. Mapping the hard decided coded bits to their corresponding symbols results in the derivation of hard decisions on the symbols which are less erroneous, which are fed back into equation (7).

In parallel, the soft values in equation (11) are subtracted by $L_e^D(c_{k,i})$ to provide extrinsic information to be processed by the channel decoder.

The technique of the present invention has been simulated in a simulation environment based on the GSM system where the payload is modulated by 8-PSK. Simulation results show that the BER at the decoder output can be improved by about 2 to 3 dB using a couple of iterations in a typical urban channel environment.

Mobile users transmitting and receiving data at high rates are likely to be located in a typical urban environment. In the simulation, therefore, the GSM channel model TU3 (3km/h mobile speed) has been simulated with and without channel hopping. The channel length is assumed to be 4 taps. The channel response is estimated by the standard channel sounding technique based on the GSM training sequence in the mid-amble of the burst. The interleaving is block rectangular and over 4 bursts. The channel code is a half rate convolutional code with constraint length seven.

Figure 4 shows the BER at the decoder output for TU3 with no frequency hopping for Turbo equalisation with three iterations. Curves 406, 404, 402, and 400 represent the BER after one, two, three, and four passes of the decoder of Figure 1 respectively. In Figure 4, it can be seen that the coded bit error rate (at BER = 10^{-5}) is improved after the third iteration by 2.3 dB compared with the BER of the first pass decoding. No frequency hopping is applied.

Figure 5 shows the BER at the decoder output for TU3 with frequency hopping for Turbo equalisation with two iterations. Curves 504, 502, and 500 represent the BER after one, two and three passes of the decoder of Figure 1 respectively. In Figure 5 frequency hopping is applied. In this

case the coded bit error rate (at BER = 10^{-5}) is improved after the second iteration by almost 3 dB in comparison to the first pass decoding.

EDGE enables a GSM system to increase the data rates by employing an 8-PSK modulation scheme. As the payload is data the BER has to be kept very low (10^{-5} ... 10^{-6}). The 8-PSK modulation scheme in EDGE requires a sub-optimum equaliser. The MMSE-BDFE is low in complexity as it is independent of the size of the symbols alphabet. Turbo equalisation can increase the performance of such a receiver structure.

In this patent application it has been shown how to incorporate *a priori* information in the MMSE-BDFE. This will help to combat the ISI and error propagation in the MMSE-BDFE. The additional computation to estimate the a posterior probability of the coded bits is kept small by operating in the log domain. The max-log approximation is efficient for DSP implementation and performs well. The simulation results show that a couple of iterations are sufficient to improve the performance of a MMSE-BDFE in conjunction with a half-rate convolutional channel encoder.

Although the MMSE-BDFE in EDGE is sub-optimum, the results show that it can benefit from an iterative equalisation and decoding scheme.

Claims

1. A method of recovering a received signal comprising the steps of: equalising the received signal, channeld decoding the equalised received signal, wherein *a priori* information of the received signal is utilised in the equalisation step.
2. The method of claim 1 wherein the equalising step is performed in a sub-optimum equaliser.
3. The method of claim 1 or claim 2 wherein the channel decoding step is performed in an *a posterior* channel decoder.
4. The method of any one of claims 1 to 3 wherein the a priori information is generated in dependence on the channel decoded received signal.
5. The method of any one of claims 1 to 4 wherein the transmitted signal is recovered in a series of iterations.
6. The method of claim 5 wherein in a first iteration the received signal is decoded without any *a priori* information.
7. The method of claim 6 wherein in n subsequent iterations the received signal is equalised using *a priori* information generated in the previous iteration.
8. The method of claim 7 wherein after the (n+1)th iteration a hard decision for the received signal is generated.
9. The method of any one of claims 7 to 8 wherein after the equalisation step the *a priori* information is removed from the equalised signal before channel decoding.
10. The method of any preceding claim wherin the *a priori* information is generated by subtracting the input of the channel decoder from the output of the channel decoder.
11. The method of any preceding claim wherein the received signal is de-interleaved after equalisation.
12. The method of claim 11, wherein the *a priori* information is interleaved prior to equalisation.
13. A method of recovering a transmitted signal comprising the steps of:

in a first iteration:

equalising the received signal in a sub-optimum equaliser;

channel decoding the equalised received signal in an *a posterior* channel decoder;

generating *a priori* information in dependence on the channel decoded received signal;

for the subsequent n iterations:

equalising the received signal in the sub-optimum equaliser utilising the a priori information from the previous iteration;

adjusting the equalised received signal by removing the a priori information therefrom;

channel decoding the adjusted equalised received signal;

wherein after the (n+1)th iteration a hard decision is determined based on the adjusted equalised received signal.

14. Circuitry for recovering a transmitted signal comprising: an equaliser for equalising the received signal; a channel decoder connected to the output of the equaliser for channel decoding the received signal; and circuitry for generating a priori information of the received signal, wherein said *a priori* information forms an input to the equaliser.

15. The circuitry of claim 14 wherein the equaliser is a sub-optimum equaliser.

16. The circuitry of claim 14 or claim 15 wherein the channel decoder is an *a posterior* channel decoder.

17. The circuitry of any one of claims 14 to 16 wherein the circuitry for generating the *a priori* information receives as an input the output of the channel decoder.

18. The circuitry of any one of claims 14 to 17 further comprising a first subtractor, wherein the first subtractor subtracts the *a priori* information at the output of the circuitry for generating the *a priori* information from the output of the eqauliser, the output of the subtractor forming the input to the channel decoder.

19. The circuitry of any preceding claim wherein the circuitry for generating the *a priori* information includes a second subtractor, the second subtractor being connected to subtract the signal at the output of the channel decoder form the signal at the input of the channel decoder, the output of the second subtractor forming the output of the circuitry for generating the *a priori* information.

20. The circuitry of any one of claims 14 to 19 further comprising de-interleaving circuitry connected to de-interleave the output of the equaliser.

21. The circuitry of claim 20 further comprising interleaving circuitry connected to interleave the input of the equaliser.

22. The circuitry of any one of claims 14 to 21 wherein the circuitry is controlled to perform a series of iterations on the received signal.

23. The circuitry of claim 22 wherein the equaliser receives a signal from the circuitry for generating the a priori information on the second and subsequent iterations.

24. A Turbo equaliser for recovering a transmitted signal comprising:

a sub-optimum equaliser connected to receive as a first input the received signal and as a second input a priori information associated with the received signal, and for outputting a *a priori* equalised received signal;

circuitry, connected to receive as a first input the equalised received signal and as a second input the a priori information, and for removing the a priori information from the equalised received signal, and for generating an equalised received signal;

an *a posterior* channel decoder connected to receive as an input the equalised received signal and for outputting a channel decoded received signal;

means connected to receive as a first input the equalised received signal and as a second input the channel decoded received signal, and for outputting the a priori information; and

a hard decision genarator having an input connected to the output of the channel decoder and an output,
wherein on a first iteration of the Turbo decoder there is no *a priori* information, and wherein on the nth iteration the hard decision on the output of the hard decision generator is obtained.

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Application No: GB 9922244.0	**Examiner:** Steven Davies
Claims searched: 1-24	**Date of search:** 15 March 2000

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Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.R): H4P PEP, PRE, PRV

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Other: Online databases: WPI, EPODOC, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X,E	GB 2341296 A	(SIEMENS) page 11, line 25 - page 13, line 14 ; Figure 3	1,14 at least
X,E	EP 0959580 A1	(LUCENT) paragraphs 0004 to 0006 ; Fig.3	1-24
X,E	EP 0948140 A1	(LUCENT) paragraphs 0006 to 0010 ; Figs. 1,2	1-24

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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